

**Clean Version of Amended Specification Paragraph**

**CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED  
SEMICONDUCTOR SURFACES**

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The paragraph beginning on page 7, line 8 is amended as follows:

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Second plate 120 of capacitor 119 is common to all of the capacitors of array 100.

Second plate 120 comprises a mesh or grid of n<sup>+</sup> poly-silicon formed in deep trenches that surrounds at least a portion of second source/drain region 110 of each pillars 104 in memory cells 102A through 102D. Second plate 120 is grounded by contact with substrate 101 underneath the trenches. Second plate 120 is separated from source/drain region 110 by gate insulator 122.

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